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Synthesis, electrical properties and transport mechanisms of thermally vacuum evaporated CdTe nanocrystalline thin films

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ABSTRACT

A stoichiometry CdTe nano-structured powder was synthesized by chemical process. Thin films of different thicknesses (40, 60, and 100 nm) of CdTe were prepared by thermal evaporation method onto silicon substrates. Current–voltage (I–V) and capacitance–voltage (C–V) characteristics of CdTe nanocrystalline thin films deposited on p-Si as heterojunction have been investigated. At low voltages, current in the forward direction was found to obey the diode equation and the conduction was controlled by thermionic emission mechanism. Also, various electrical parameters were determined from the I–V and C–V analysis. The thickness dependence of the obtained capacitance–voltage (C–V) characteristics was also considered.

1. Introduction

Metal–semiconductor (MS) contacts have great importance both in modern electronic applications and understanding solid-state electronic devices. Metal–semiconductor contacts have been specially used as gate electrodes of a field-effect transistor (MESFET), the drain and source contacts in metal-oxide-semiconductor field-effect transistor (MOSFET) which is the most important device for very-large-scale integrated circuits such as microprocessors and semiconductor memories, the electrodes for high-power IMPATT oscillators, and fabrication of photodetectors and solar cells [1–3]. The current-transport process and device technology of MS structures have been reviewed by Rhoderick [4] and by Rideout [5]. The current transport in MS contacts is mainly due to majority carriers in contrast to p–n junctions where the minority carriers are responsible. MS contacts are assumed to be abrupt junction with a fixed barrier height with respect to the classical model. The Schottky barrier height is an important parameter which determines the electrical characteristics of MS contacts and has crucial importance for successful operation of semiconductor devices [1–6]. Schottky barrier height is defined as the difference between the edge of the respective majority-carrier band of the semiconductor and the Fermi level at the interface. Most of the experimental and theoretical studies have been made on the nature and formation of the barrier height at MS contacts.

The current–voltage (I–V) characteristics of real Schottky barrier diodes have difference from the prediction of thermionic emission theory (TET). TET assumes that the junction is abrupt with fixed Schottky barrier height (SBH) [7–9]. Furthermore, certain experimental data analyzed using TET cannot be well understood. For example, ideality factor is larger than unity and this indicates that the barrier heights change as a function of applied voltage. Another commonly observed anomaly is the dependence of SBH on the measurement technique. SBHs measured by the C–V technique often significantly exceed that derived from I–V and photo-response (PR) techniques. These deviations have been explained by assuming the presence of the lateral barrier height inhomogeneities [7–11]. Some common causes for the barrier heights difference have been mentioned in the literature, such as contamination in the interface, an intervening insulator layer, deep impurity levels or edge leakage currents [1–4]. Some researchers have explained the discrepancy by the existence of two regions of contact area, each having a different barrier height [11,12].

Cadmium telluride (CdTe) has been recognized as a very promising material for thin-film solar cells. CdTe is a II–VI compound semiconductor with a direct optical bandgap of ~1.5 eV that is nearly optimally matched to the solar spectrum for photovoltaic (PV) energy conversion. CdTe also has a high

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absorption coefficient, $>5\times10^5$/cm, which means that ~99% of photons with energy greater than the bandgap (E_g) can be absorbed within 2 μm of CdTe film. Small-area CdTe cells with efficiencies of more than 15% have been developed [13,14]. Here we have mainly focused on the preparation of nanocrystalline CdTe because the nanostructured semiconductor materials have attracted much attention due to their unique electrical, magnetic and optical properties. CdTe is one of the most promising photovoltaic materials for the thin film solar cells due to its direct band gap matching to the solar energy spectrum and high absorption coefficient [15–19]. It is expected that nanostructured CdTe thin films would exhibit unusual charge carrier dynamics, improved collection of the photogenerated carriers and the enhanced solar conversion efficiency. It is because, first, due to multiple reflections, the effective optical path for absorption is much larger than the actual film thickness. Second, light generated electron and holes need to travel over a much shorter path and thus recombination losses are greatly reduced. As a result, the absorber layer thickness in nanostructured solar cells can be as thin as 150 nm instead of several micrometers in the traditional thin film solar cells [20]. Third, the energy band gap of various layers can be tailored to the desired design value by varying the size of nanoparticles. This allows for more design flexibility in the absorber and window layers in the solar cells [21].

In the present work, CdTe nanocrystalline thin film was prepared by thermal evaporation for CdTe nanocrystalline powder which prepared by chemical process onto silicon wafer substrates at room temperature. The optical and structural properties of CdTe nanocrystalline thin films as well as morphological characterization of CdTe powder were reported in our previous work [22]. The analysis of the CdTe nanocrystalline thin film has been done using current–voltage and capacitance–voltage characteristics at different temperature in order to determine structural and electrical properties, respectively.

2. Experimental section

Nanocrystalline CdTe powder was synthesized by chemical process as reported in previous work [22]. Thin films of thickness 40, 60, and 100 nm were prepared by using an Edward Coating Unit E-306, onto silicon wafer substrates at room temperature on a base pressure of 10^{-6} Torr using molybdenum boat. The powder was placed in a high curved wall molybdenum boat and slowly applied voltage and evaporation rates were in the range 0.05 to1 nm.

The substrates were thoroughly cleaned in a detergent solution and then in a chromic acid and finally, cleaned using trichloroethylene. Double distilled water was used throughout in different stages of cleaning. To avoid the fractionation [23–25] of the alloy during evaporation and, thereby, to ensure the correct average composition of the films formed, a high deposition rate was used to prepare the studied films. The thickness of the films was measured by using a quartz crystal monitor Edward model FTM 7. The earthed face of the crystal monitor was facing the source and was placed at the same height as the substrate. The evaporation was controlled by using the same FTM 7 quartz crystal monitor.

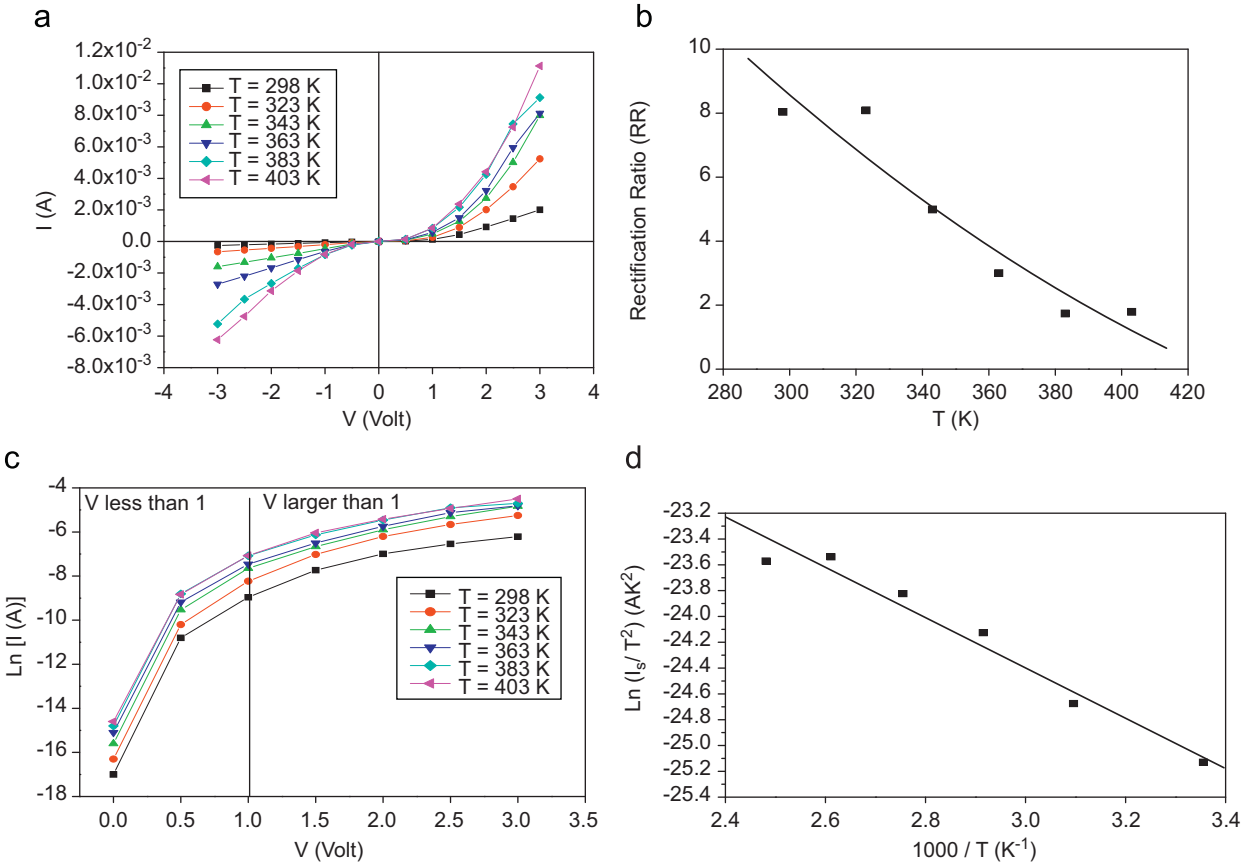

Fig. 1. (color online) (a) *I–V* characteristics of CdTe/p-Si heterojunction at different temperatures with film thickness=40 nm, (b) the relation between rectification ratio (RR) and temperature with film thickness=40 nm, (c) *I–V* characteristics of CdTe/p-Si heterojunction at different temperatures with film thickness=40 nm, (d) plot of (I_s/T^2) versus 1/*T*.

The dark current–voltage (I–V) measurements were performed at different temperatures by a high impedance programmable Keithley 617 source meter. The dark capacitance–voltage measurements were performed at different temperatures by maintaining a constant fixed frequency at 1 MHz, using a computerized capacitance–voltage system consisting of the 410 C–V meter via model 4108 C–V interface. The temperature was measured directly by means of chromel–alumel thermocouple connected to hand-held digital thermometer, maintaining constant fixed-frequency switching at 1 MHz for low output ripple and noise. Electrodes for electrical measurements were formed by evaporating gold on both sides with a thickness on range 30–40 nm. In order to make sure of the reservation of the stoichiometry, EDAX measurements were carried out (see Supplementary material).

3. Results and discussion

3.1. Current–voltage characteristics of CdTe nanocrystalline thin film

It is known that material quality, electrical and optical properties of the films strongly depend on the film thickness and show large change around the film thickness. For example resistivity increases as the film thickness increases implying that the most films conduct due to the highest carrier concentration. In other words, as the film thickness increases, the resistivity of the films increases since it is inversely proportional to the carrier concentration [25]. The particle size variation plays significant rules in affecting the properties of materials. It is expected that as the thickness changes there will be a particle size changes. It is obvious that the surface morphology of the films varies with the film thickness whereas thickness become smaller smooth morphology can take place [25].

The I–V characteristics of the CdTe/p-Si heterojunction at different temperatures in the range 298–403 K and with different thickness values are shown in Figs. 1–3. This figure illustrates a rectifying behavior for the obtained junction, i.e., while the reverse current shows weak bias voltage dependence, the forward current increases exponentially with the voltage increase. The rectification ratio, RR obtained at ± 3 V for each temperature was listed in Table 1. As observed, the high RR values may be attributed to the formation of potential barrier in the CdTe/p-Si heterojunction. The measurements of the physical quantities such as saturation current, barrier height and the ideality factor of the CdTe/p-Si heterojunction are made using the well-known current–voltage relation described in the thermionic emission model [26]:

$$I = AA^*T^2\exp\left(-\frac{q\Phi_{eff}}{kT}\right)\exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

where A is the contact area, A^* is the Richardson constant, q is the electronic charge, T is the temperature, n is the ideality factor which measure the conformity of the diode to pure thermionic emission and Φ_{eff} is the effective barrier height.

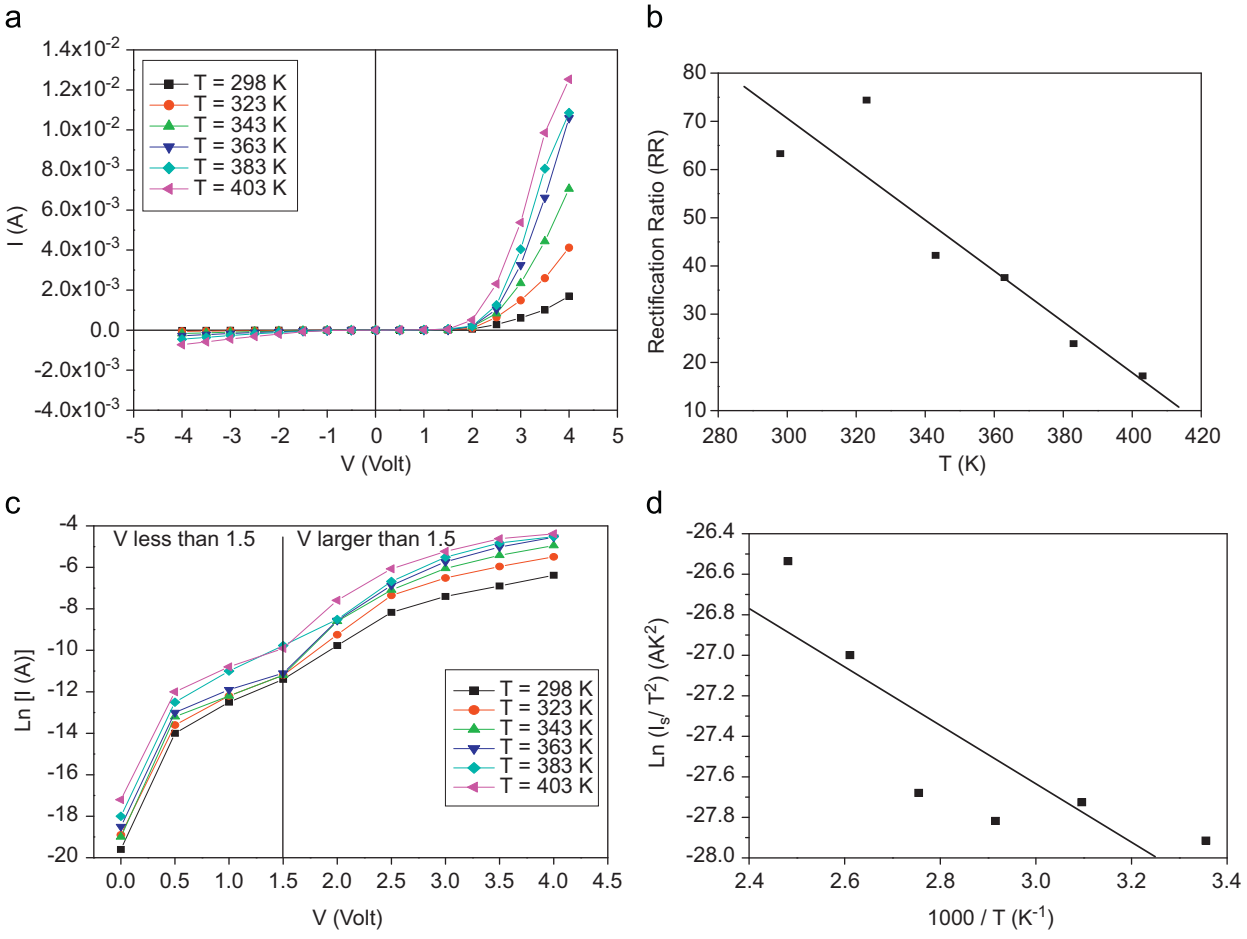

Fig. 2. (color online) (a) I–V characteristics of CdTe/p-Si heterojunction at different temperatures with film thickness = 60 nm, (b) the relation between rectification ratio (RR) and temperature with film thickness = 60 nm, (c) I–V characteristics of CdTe/p-Si heterojunction at different temperatures with film thickness = 60 nm, (d) plot of (I_s/T^2) versus 1/T.

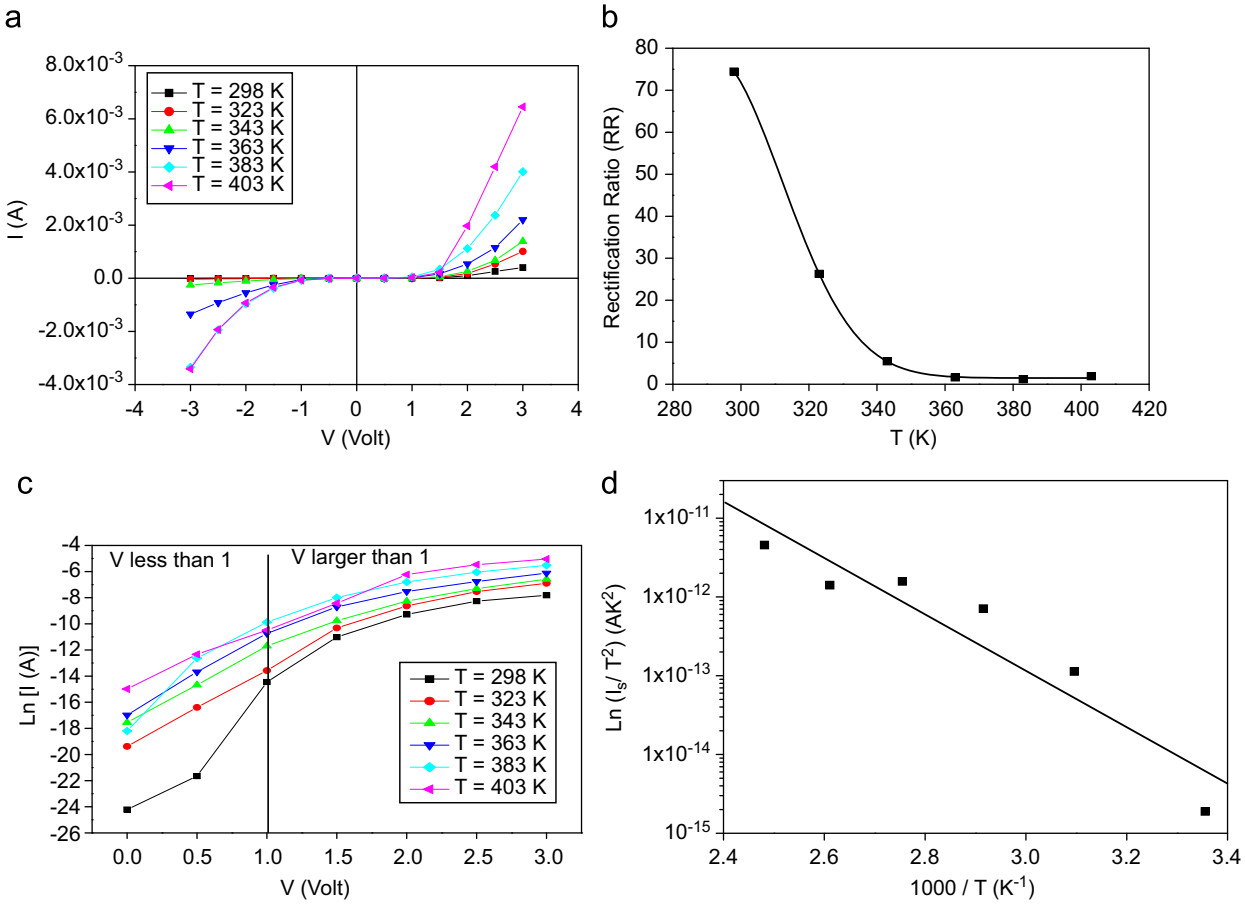

Fig. 3. (color online) (a) *I–V* characteristics of CdTe/p-Si heterojunction at different temperatures with film thickness = 100 nm, (b) the relation between rectification ratio (RR) and temperature with film thickness = 100 nm, (c) *I–V* characteristics of CdTe/p-Si heterojunction at different temperatures with film thickness = 100 nm, (d) plot of (I_s/T^2) versus $1/T$.

Table 1
Parameters deduced from *I–V* characteristics at different temperatures with different film thickness.

T (K)	Film thickness = 40 nm				Film thickness = 60 nm				Film thickness = 100 nm			
	RR	*N*	I_0 (A)	Φ_{eff}	RR	*n*	I_0 (A)	Φ_{eff}	RR	*n*	I_0 (A)	Φ_{eff}
298	8.04	12.71	1.08×10^{-6}	0.449	63.31	13.32	6.69×10^{-8}	0.521	74.45	6.72	1.68×10^{-10}	0.675
323	8.09	11.35	2.01×10^{-6}	0.474	74.42	11.73	9.49×10^{-8}	0.559	26.29	8.36	1.18×10^{-8}	0.618
343	4.99	11.13	3.91×10^{-6}	0.487	42.23	10.57	9.76×10^{-8}	0.597	5.45	9.27	8.33×10^{-8}	0.602
363	3.00	10.95	5.94×10^{-6}	0.507	34.62	9.95	1.26×10^{-7}	0.627	1.62	9.01	2.08×10^{-7}	0.612
383	1.74	10.66	8.79×10^{-6}	0.525	23.92	9.98	2.76×10^{-7}	0.639	1.19	7.81	2.07×10^{-7}	0.649
403	1.79	10.13	9.42×10^{-6}	0.554	17.23	9.76	4.86×10^{-7}	0.657	1.89	8.43	7.39×10^{-7}	0.642

The experimental values of Φ_{eff} and n were determined from the intercept and slope of the straight line region of the semilog-forward bias *I–V* plot at each temperature with different film thickness, respectively, and listed in Table 1. As observed, n is considerably high in the lower temperature region. As the operating temperature is raised, the temperature sensitivity of n is gradually reduced to a much lower value. The model of an inhomogeneous Schottky diode with a few low-Schottky barrier patches provides the plausible explanation for the experimental observations. As already discussed, in the lower temperature regime, the resultant current through the Schottky junctions were determined by the current component flowing through the localized low-barrier height regions. As a consequence, the ideality factor derived from the *I–V* characteristics deviates far from unity. The high series resistance in the low-Schottky barrier height patches also influences the value of n in this temperature range. With the increase of the operating temperature, the current transport is gradually dominated by the homogeneous region of the Schottky contacts with higher barrier height and lower series resistance. This is reflected in the improved ideality factor of the junctions at higher temperature.

Fig. 4 shows a plot of Φ_{eff} vs. n at each temperature. The obtained linear relationship of the heterojunction can be explained by lateral inhomogenities of the barrier height. The barrier height inhomogenity for CdTe/p-Si may be attributed to the considerable mismatch in the lattice constant and thermal expansion coefficient between CdTe and p-Si resulting in high tensile stress at the interface, that introduce defects such as misfit dislocations, stacking faults and antiboundaries, which are likely the origin of localized inhomogenity of the barrier height [27].

From the above discussion it can be realized that the true barrier height can be obtained at high temperature. The effective barrier

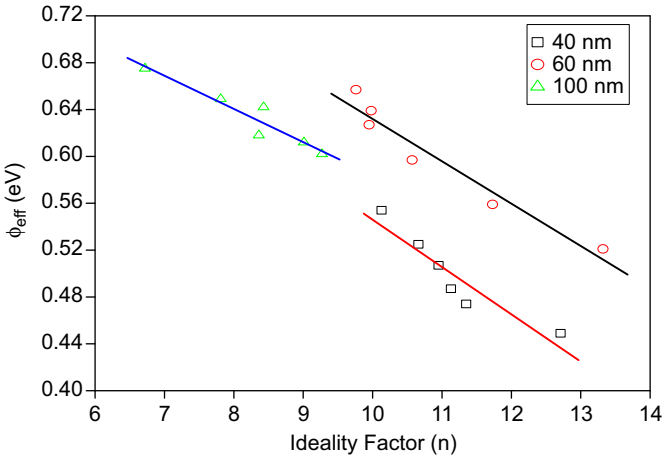

Fig. 4. Effective barrier height Φ_{eff} vs. ideality factor, n at different film thickness (40, 60, and 100 nm).

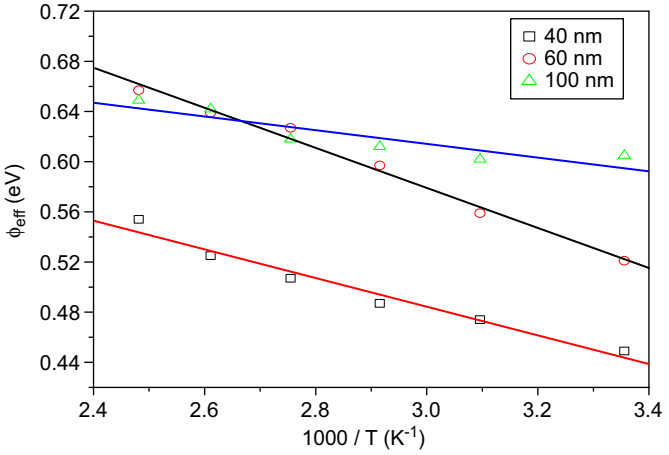

Fig. 5. (color online) Temperature dependence of effective barrier height at different film thickness (40, 60, and 100 nm).

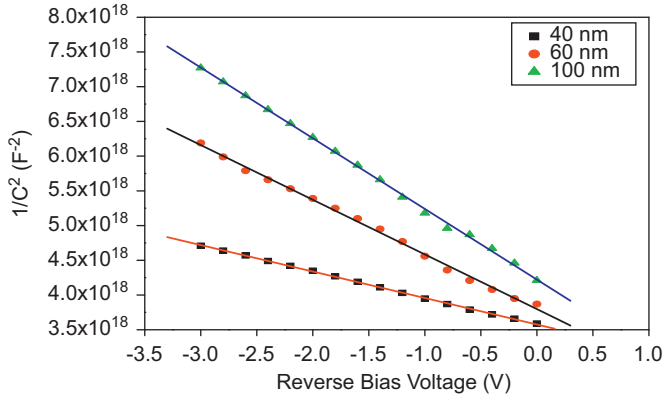

Fig. 6. (color online) Plot of $1/C^2$ vs. reverse bias voltage at room temperature with different film thickness (40, 60, and 100 nm).

height, measured from the current–voltage characteristics, at relatively low temperatures are only apparent values. This argument is further substantiated by the determination of Φ_b from capacitance–voltage measurement, which gives the arithmetic mean of Φ_b, weighed by the area fraction, for the barrier regions.

Lateral fluctuations of the barrier height are commonly observed in Schottky contacts and could be the contributor for such a behavior. A plot of effective barrier height Φ_{eff} vs. inverse temperature is shown in Fig. 5. The lateral fluctuations could be modeled by a Gaussian distribution of barrier heights with standard deviation σ_s around a mean value Φ_b. The effective barrier height is related to the mean barrier height by a relation [28]:

$$\Phi_{eff} = \Phi_b - \frac{q\sigma_s^2}{2kT}. \tag{2}$$

The mean barrier height, Φ_b and the standard deviation, σ_s can be determined, respectively from the intercept and slope of Fig. 5 in accordance with Eq. (2). From the linear fit, the mean barrier height Φ_b and σ_s were obtained to be (0.827 and 0.141 eV), (0.999 and 0.166 eV), and (0.778 and 0.097 eV) for thickness film=40, 60, and 100 nm, respectively. By comparing Φ_b (at T=0 K) and σ_s parameters, it is found that the standard deviation, which is the measure of barrier height homogeneity is ~13.5% of the mean barrier height.

Table 2
Parameters deduced from C–V characteristics at room temperature with different film thickness.

Film thickness (nm)	C–V characteristics		
	N ($\times 10^{20}$ cm^{-3})	V_b (V)	Φ_b (eV)
40	14.09	0.74	0.121
60	6.82	0.37	0.303
100	5.28	0.17	0.679

3.2. Capacitance–voltage characteristics of CdTe nanocrystalline thin film

The capacitance–voltage characteristics of CdTe/p-Si heterojunction were measured at a sufficiently high frequency (1 MHz). This frequency is high enough to neglect the dielectric relaxation process in CdTe nanocrystalline film [29] and get information on the depletion region extended in the p-Si side.

The charge at the interface states cannot follow the ac signal. This will occur when the time constant is too long to permit the charge to move in and out of the states in response to an applied signal [2,28,30]. Thus, for CdTe/p-Si heterojunction, the depletion layer capacitance can be expressed as follows:

$$\frac{1}{C^2} = \frac{2(V_b + V_r - kT/q}{q\varepsilon_s\varepsilon_0 A^2 N} \tag{3}$$

where V_b is the built-in voltage determined from the extrapolation of the C^{-2}–V plot to the voltage axis, V_r is the reverse voltage, A is the area of the diode, ε_s is the static dielectric constant and N_i is the net carrier concentration. The N is related to the slope of C^{-2} vs. V curve and can be obtained from the expression:

$$N = \frac{2}{q\varepsilon_s\varepsilon_0 A^2}\left[\frac{1}{d(C^{-2})/dV}\right]. \tag{4}$$

The barrier height deduced from capacitance is then obtained from

$$\Phi_b^{C-V} = V_b + V_n + \frac{kT}{q} - \Delta\phi \tag{5}$$

where V_n referred to as the Fermi level potential, and given by $V_n = kT/q[\ln(N_v/N)]$. Thus, Eq. (5) can be rewritten by neglecting the image-force barrier lowering ($\Delta\phi$) as

$$\Phi_b^{C-V} = V_b + \frac{kT}{q}\left[1 + \ln\frac{N_v}{N}\right] \tag{6}$$

where N_v ($=1.8\times10^{19}$ cm^{-3}) is the effective density of states in the valence band for p-Si.

Fig. 6 shows the reverse bias C^{-2}–V plots for the n-CdTe/p-Si as a function of film thickness at room temperature for a modulation frequency of 1 MHz. The capacitance of the diode in the range of 0.0 to −3.0 V has increased with increasing film thickness as can be seen from Fig. 6. As observed, linear C^{-2} −V plots were obtained for the whole investigated film thickness range. This indicates the presence of the abrupt heterojunction for the prepared heterojunction Furthermore, the linear behavior of the curves can be explained by the fact that the interface states and the inversion layer charge cannot follow the ac signal at 1 MHz and consequently do not contribute appreciably to the diode capacitance. The V_b and N values are obtained from the intercept and the slope of the extrapolated C^{-2}–V lines with the V_r axis, respectively, and listed in Table 2. Then, the values of Φ_b^{C-V} are calculated by using Eq. (6).

4. Conclusion

The I–V and C–V characteristics were investigated at different temperatures of the CdTe/p-Si structure. The values of the ideality factor, series resistance and barrier height calculated by using different methods were compared. An accurate determination of CdTe/p-Si device parameters was obtained by taking into account the applied voltage drop across the interfacial layer (V–IR$_s$). The I–V results at various temperatures of CdTe/p-Si heterojunction were fitted to a model of a Gaussian distribution of the barrier heights, suggesting that the barrier at the interfaces is not spatially uniform. The unexpectedly low Richardson's constant obtained, and the barrier height linear correlation with ideality factor has been attributed to inhomogeneities that prevail at the CdTe/p-Si interface. The corrected value of the Richardson's constant was found to be in good agreement with theory. Finally, it can be speculated from the diode parameters obtained by I–V and C–V techniques that the spatial inhomogeneities of the barrier height is an important factor and could not be ignored in the analysis of temperature dependent electrical characterization of the CdTe/p-Si structures.

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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.ssc.2012.05.029.

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